We claim:

1. A dual mode processor array comprising:

a control processor; and

at least one processing element sharing a single set of function units,

said dual mode processor acting as a processing element in a first mode of operation, and acting as a controlling element in a second mode of operation.

2. The apparatus of claim 1 wherein the control processor comprises a register file and a plurality of functional units, one of the plurality of functional units comprising an instruction sequencer for fetching instructions.

3. The apparatus of claim 1 wherein the processing element comprises a register file and a plurality of functional units, the plurality of functional units not including an instruction sequencer.

4. The apparatus of claim 1 wherein the dual mode processor is connected with a plurality of processing elements by an interconnection bus to form a processing array.

5. The apparatus of claim 4 wherein the dual mode processor and the plurality of processing elements further comprise register files and the interconnection bus is utilized as a direct communication path between any processing element register file and any register file in the dual mode processor utilized in said second mode.

6. The apparatus of claim 1 wherein the control processing of the dual mode processor further comprises instruction fetching, the dual mode processor and the processing element being operable to decode each instruction and to examine a mode of operation bit in the instruction to determine the mode of operation in which the instruction should be executed for instruction execution of control type instructions and instruction execution of PE type instructions.

7. The apparatus of claim 4 further comprising a register file selection mechanism.

8. The apparatus of claim 4 wherein the dual mode processor and the processing elements further comprise a plurality of register files and the plurality of register files of the dual mode processor are organized in banks.

9. The apparatus of claim 8 further comprising a register file bank selection mechanism.

10. The apparatus of claim 1 wherein the dual mode processor further comprises an instruction sequence which fetches instructions, the control processor and the processing element being operable to decode each instruction and to examine a most significant bit in the

instruction to determine the mode of operation.

11. A method of operating an array comprising a dual mode processor and a plurality of processing elements connected to the dual mode processor with an interconnection bus, the method comprising the steps of:

operating the dual mode processor as one of the processing elements in the dual mode array to participate in the execution of single instruction multiple data instructions in a first mode of operation; and

operating the dual mode processor as a controlling element for the array to execute non-array instructions in a second mode of operation.

12. The method of claim 11 further comprising the step of:

determining the mode of operation of the dual mode processor based upon an examination of a mode of operation bit in an instruction.

13. The method of claim 11 further comprising the step of:

determining the mode of operation of the dual mode processor based upon an examination of the most significant bit in the destination register selection field of an instruction.

14. The method of claim 11 further comprising the step of:

selecting a register file in the dual mode processor utilizing the most significant bit of the register selection fields of an instruction.

15. The method of claim 11 further comprising the steps of:

organizing register files in the dual mode processor in banks; and

selecting a register file bank in the dual mode processor utilizing a register file bank selection mechanism.

16. An apparatus for concurrently executing controller SISD instructions and SIMD processing element instructions comprising:

a combined controller and processing element;

at least two simplex instructions each containing a mode of operation bit; and

very long instruction word (VLIW) containing said at least two simplex instructions.

17. The apparatus of claim 16 further comprising a very long instruction word (VLIW) decode and control logic block.

18. The apparatus of claim 17 further comprising a sequence processor register file and a processing element register file connected to receive write enable control signals from the VLIW decode and control logic block.

19. The apparatus of claim 18 further comprising at least two multiplexers to

control the source data path from said register files to inputs of functional units of the combined controller and processing element.

20. The apparatus of claim 16 wherein the combined controller and processing element is connected by an interconnection bus to a plurality of processing elements in a manifold array processing architecture.